ABSTRACT

According to one embodiment, the memory circuit comprises a memory sector having a plurality of memory cells. Each of the plurality of memory cells has a gate connected to a corresponding word line, where each corresponding word line is further connected to an output of a corresponding decoding circuit. Each corresponding decoding circuit receives a corresponding vertical word line signal, a corresponding global word line signal, and a corresponding sector supply voltage. The corresponding sector supply voltage is capable of supplying an erase voltage, such as -9 V for a negative gate erase memory device, for example. With this arrangement, the corresponding decoding circuit is capable of selectively excluding the corresponding word line from receiving the erase voltage during the erase operation.

Figure 3 should accompany the Abstract.